Homework # 6

Due Tuesday, March 13, 2001, at 5:00 PM at the TA office, Moore 311

Collaboration and/or discussion are not allowed on this homework set, however, you can discuss it with the lecturer/TA.

1. **Lower Bounds on Non-Layered LT Circuits for Symmetric Functions**
   A symmetric function $f(x_1, x_2, \cdots, x_n)$ can be described by a vector of length $n+1$ that we call $V(f) = (v_0, v_1, \cdots, v_n)$ with

   $$v_i = \begin{cases} 1 & \text{if for } |X| = i \ f(X) = 1 \\ 0 & \text{otherwise} \end{cases}$$

   Now assume that you are given a symmetric function f with $V(f)$ consisting of k intervals of 1's. In HW #2 problem 4 you proved that f can be implemented by a depth-2 *non-layered* circuit with at most $k+1$ elements. In the construction there you used TH elements in the first layer.

   Prove that this implementation of symmetric functions is of optimal size, assuming one uses TH elements in the first layer.

2. **Lower Bounds for Product and Sorting**
   In class we learned that *Product* (multiplication of two integers of n bits each) and *Sorting* (sorting of n integers with n bits each) are in $\hat{LT}_3$. Here we will prove that *Product* and *Sorting* are not in $\hat{LT}_2$. Namely, depth 3 is optimal for both functions.

   Let the Inner-Product-Mod 2 (IP2) be the following function that is defined for n even.

   $$IP2(x_1, x_2, \cdots, x_n) = (x_1 \wedge x_2) \oplus (x_3 \wedge x_4) \oplus \cdots \oplus (x_{n-1} \wedge x_n)$$

   For example, for $n = 4$,

   $$IP2(x_1, x_2, x_3, x_4) = (x_1 \wedge x_2) \oplus (x_3 \wedge x_4)$$

   Assume that $IP2 \notin \hat{LT}_2$.

   Prove by the technique of reduction that:

(a) $Product \notin \hat{LT}_2$.

(b) $Sorting \notin \hat{LT}_2$.

3. **Cyclic Combinational Circuits**

In class we discussed combinational versus sequential circuits. Combinational circuits are "memoryless", i.e., the outputs depend only on the present values of the inputs. Sequential circuits have "memory", i.e., the outputs may depend on the past as well as present input values.

(a) In class we analyzed the circuit shown below, due to Rivest. It has three inputs a, b and c; six gates, each with fan-in 2, arranged in a single cycle; and six outputs, one from each gate. We argued that the circuit is combinational and produces the output functions shown. Note that each function depends on all three input variables. We argued that any acyclic circuit of fan-in 2 gates that implements the same output functions must have at least seven gates.

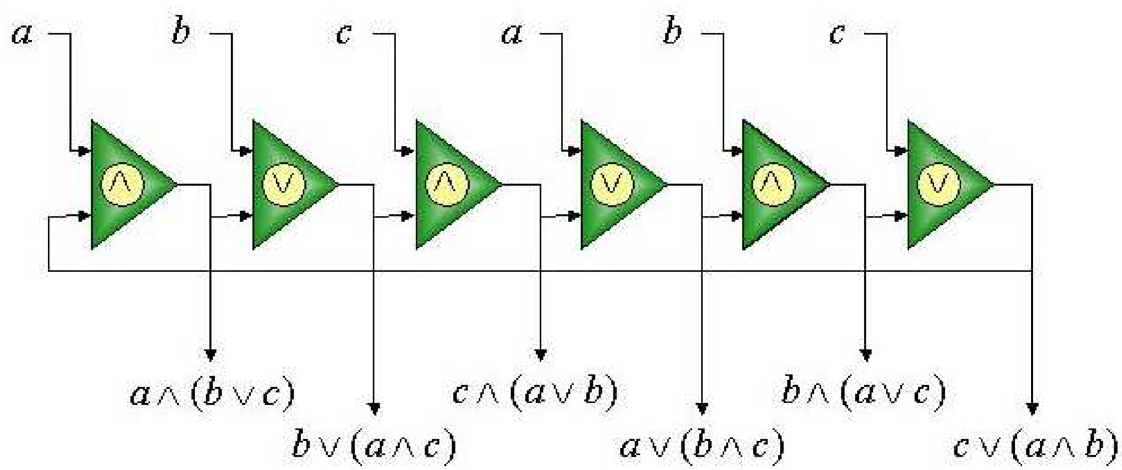

Figure 1: Rivest circuit

Generalize the Rivest circuit in the following way.

i. Construct a circuit with six inputs and six fan-in 3 AND/OR gates such that each gate produces an output function that depends on all six input variables. What is the minimum number of fan-in 3 gates that would be required for an acyclic circuit that implements the same six functions? Justify your answer.

ii. Construct a circuit with $n(d-1)$ inputs and $2n$ fan-in d AND/OR gates, for $n \geq 3$, n odd, and $d \geq 2$, such that each gate produces an output function that depends on all $n(d-1)$ input variables. What is the minimum number of fan-in d gates that would be required for an acyclic circuit that implements the same $2n$ functions? Justify your answer.

(b) Construct a circuit consisting of six fan-in 2 AND/OR/NAND/NOR gates that implements six of the following eight functions:

$$\begin{aligned}
f1 &= b + abc \\
f2 &= bc + abc \\
f3 &= 1 + ab + abc \\
f4 &= a + bc + abc \\
f5 &= c + bc + abc \\
f6 &= ac + bc + abc \\
f7 &= 1 + a + ab + abc \\
f8 &= 1 + ab + bc + abc
\end{aligned}$$

(Multiplication represents AND, addition XOR, and 1 "true".) Prove that your circuit is combinational.